# CLAIMS

What is claimed is:

1. A system for mitigating line-edge roughness on a semiconductor device, comprising:

a non-lithographic shrink component that facilitates mitigating line-edge roughness; and

a trim etch component that facilitates achieving a target critical dimension.

2. The system of claim 1, further comprising a monitoring component that monitors information associated with at least one of critical dimension and line-edge roughness on a photoresist.

3. The system of claim 2, the monitoring component comprising at least one of a scatterometry system and a Scanning Electron Microscopy system.

4. The system of claim 1, further comprising a processor that processes data associated with at least one of critical dimension and line-edge roughness on a photoresist.

5. The system of claim 4, the processor comprising an artificial intelligence component that facilitates making inferences regarding at least one of mitigating line-edge roughness and achieving target critical dimension on a photoresist.

6. The system of claim 5, the artificial intelligence component comprising at least one of a support vector machine, a neural network, an expert system, a Bayesian belief network, fuzzy logic, and a data fusion engine.

7. The system of claim 1, further comprising a memory component that stores data associated with at least one of mitigating line-edge roughness and achieving target critical dimension on a photoresist.

8. The system of claim 7, the memory component comprising at least one of volatile and non-volatile memory.

9. The system of claim 1, the non-lithographic shrink component comprising at least one of a thermal reflow component, a Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS™) component, and a Shrink Assist Film for Enhanced Resolution (SAFIER) component.

10. A method for mitigating line-edge roughness on a semiconductor device, comprising:

determining whether line-edge roughness is extant on a patterned photoresist;

employing a non-lithographic shrink technique to mitigate line-edge roughness; and

employing a trim etch technique to compensate for any increase in critical dimension between lines on a photoresist.

11. The method of claim 9, further comprising processing information associated with photoresist line status.

12. The method of claim 9, further comprising making inferences regarding photoresist line status.

13. The method of claim 9, further comprising storing information associated with photoresist line status.

14. The method of claim 9, the presence of line-edge roughness is determined *via* employing at least one of a scatterometry technique and Scanning Electron Microscopy.

15. The method of claim 9, the non-lithographic shrink technique comprising at least one of a thermal reflow technique, a Resolution Enhancement Lithography Assisted by Chemical Shrink (RELACS™) technique, and a Shrink Assist Film for Enhanced Resolution (SAFIER) technique.

16. The method of claim 9, further comprising generating feedback data that facilitates controlling at least one parameter associated with at least one of LER mitigation and critical dimension maintenance.

17. A system for mitigating line-edge roughness on a semiconductor device, comprising:

means for mitigating line-edge roughness; and

means for trimming excess resist material to achieve a target critical dimension.

18. The system of claim 17, further comprising means for monitoring photoresist line status.

19. The system of claim 17, further comprising means for processing information associated with photoresist line status.

20. The system of claim 17, further comprising means for storing information associated with photoresist line status.

21. The system of claim 17, further comprising means for making inferences related to photoresist line status.

22. The system of claim 17, the means for mitigating line-edge roughness comprising means for performing a non-lithographic shrink technique.

23. The system of claim 17, the means for trimming excess resist material comprising means for performing a trim etch.